Docket No.: 10046.0155
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Holger Sedlak et al.

Application No.: 10/701,058 Confirmation No.: 5559

Filed: November 4, 2003 Art Unit: 2836

For: FREQUENCY REGULATING CIRCUIT Examiner: D. M. Parries

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is filed with two months of the Notice of Appeal filed concurrently herewith.

This Appeal Brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

XIII. Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is: Infineon Technologies AG.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1, 3, 4, 6, 7, and 9 are rejected and are under appeal.

IV. STATUS OF AMENDMENTS

No Amendments After Final Rejection have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The subject matter of each independent claim is described in the specification of the instant application. The page and line numbers and reference numbers below are examples of where the claimed features may be found in the specification; the page and line numbers and reference numbers do not necessarily represent an exhaustive list of all portions of the application providing support for the claimed features.

A. Independent claim 1:

Independent claim 1 is directed to a frequency regulating circuit for the current-consumption-dependent clock supply [4] of a circuit configuration [1]. See Figures 1 and 2.

A current measuring device [2] measures an instantaneous current consumption of the circuit configuration. [Abstract.]

A means for comparing [12] compares the instantaneous current measured by the current measuring device [2] with a definable threshold value [page 5, lines 18-20].

A controllable clock supply circuit [4] has an output [6] to be connected to a clock input [11] of the circuit configuration [1; page 7, lines 5-7]. A clock generator [7] generates a clock signal with clock pulses, and generates a constant maximum internal frequency [page 7, lines 25-26]. A pulse filter [8] filters clock pulses from the clock signal from the clock generator [7], said pulse filter [8] including a control input, a filtered clock signal being provided to the output [6] [page 7, line 26, though page 8, line 5].

A control device [3] is connected to the clock supply circuit [4] and drives the clock supply circuit [4] based upon the measured current consumption, the control device [3] provides a control signal to the control input of the pulse filter [8] when the means for comparing [12] determine that the instantaneous current consumption exceeds the definable threshold value [page 7, lines 1-4; and page 8, lines 7-10].

The pulse filter [8] suppresses at least one clock pulse of the clock signal generated by the clock signal generator [7], in response to the control signal at the control input, such that the control device [3] adjusts the clock frequency instantaneously and non-incrementally to provide at the output [6], at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit. [Page 7, line 23, through page 8, line 5.]

B. Independent claim 4:

Independent claim 4 is directed to a frequency regulating circuit for the current-consumption-dependent clock supply [4] of a circuit configuration [1]. See Figures 1 and 2.

A current measuring device [2] measures an instantaneous current consumption of the circuit configuration [1]. [Abstract.]

A means for comparing [12] the instantaneous current measured by the current measuring device [2] with a definable threshold value [page 5, lines 18-20].

A controllable clock supply circuit [4] has an output [6] to be connected to a clock input [11] of the circuit configuration [1; page 7, lines 5-7]. A generator [7] generates a constant maximum internal frequency [page 7, lines 25-26]. A pulse filter [8] is connected to at least one of the clock generator [7] and the output [7], and filters clock pulses from the clock signal from the clock generator [7], the pulse filter [8] including a control input, a filtered clock signal being provided to the output [page 7, line 26, though page 8, line 5].

A control device [3] is connected to the clock supply circuit [4] and drives the clock supply circuit [4] based upon the measured current consumption. The control device [3] is programmed to provide a control signal to the control input of the pulse filter [8] when the means for comparing [12] determines that the instantaneous current consumption exceeds the definable threshold value. [Page 7, lines 1-4; and page 8, lines 7-10.]

The pulse filter [8] suppresses at least one clock pulse of the clock signal generated by the clock signal generator [7], in response to the control signal at the control input, such that, the control device [3] adjusts the clock frequency instantaneously and non-incrementally to provide at the output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit [1]. [Page 7, line 23, through page 8, line 5.]

C. Independent claim 7:

Independent claim 7 is directed to a frequency regulating circuit for the current-consumption-dependent clock supply of a circuit configuration [1]. See Figures 1 and 2.

A current measuring device [2] measures an instantaneous current consumption of the circuit configuration [1]. [Abstract.]

A means for comparing [12] compares the instantaneous current measured by the current measuring device [2] with a definable threshold value [page 5, lines 18-20].

A controllable clock supply circuit [4] has an output to be connected to a clock input of the circuit configuration [1; page 7, lines 5-7]. A clock generator [7] generates a clock signal with clock pulses, and generates a constant maximum internal frequency [page 7, lines 25-26]. A pulse filter [8] is connected between the clock generator [7] and the output [6]. The pulse filter [8] has a control input [page 7, line 26, though page 8, line 5].

A control device [3] is connected to the clock supply circuit [4] and drives the clock supply circuit [4] based upon the measured current consumption. The control device [3] is programmed to provide a control signal to the control input of the pulse filter [8] when the means for comparing [12] determines that the instantaneous current consumption exceeds the definable threshold value. [Page 7, lines 1-4; and page 8, lines 7-10.]

The pulse filter [8] filters out at least one clock pulse of the clock signal generated by the clock signal generator [7], in response to the control signal at the control input, such that, the control device [3] adjusts the clock frequency instantaneously and non-incrementally to provide at the output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit. [Page 7, line 23, through page 8, line 5.]

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1, 3, 4, 6, 7, and 9 have been erroneously rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.[1]

B. Whether claims 1, 3, 4, 6, 7, and 9 have been erroneously rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

[1] In related objections, the specification has been objected to as allegedly failing to provide proper antecedent basis for adjusting the clock frequency non-incrementally, and the drawings are objected to for allegedly not showing this feature. Applicant reserves the right to address these objections after the related rejections are resolved.

C. Whether claims 1, 3, 4, 6, 7, and 9 have been erroneously rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

D. Whether claims 1, 3, 4, 6, 7, and 9 have been erroneously rejected under 35 U.S.C. 103(a) as being unpatentable over Durham et al. (US 5,761,517; hereinafter "Durham") in view of Wang (US 5,943,203).

VII. ARGUMENT

A. Whether claims 1, 3, 4, 6, 7, and 9 have been erroneously rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

It is the Examiner's position that the specification does not explicitly teach adjusting the clock frequency non-incrementally.

Appellant respectfully disagrees. One of ordinary skill in the art reading the application as a whole understands that the application as originally filed describes a clock frequency that is adjusted non-incrementally.

The application describes a frequency regulating circuit that compares an instantaneous current consumption with a threshold value. If the instantaneous current consumption is lower than the threshold value, individual clock pulses pass through, and if the instantaneous current consumption is higher, the individual clock pulses are suppressed. The frequency regulating circuit adjusts the clock frequency immediately.

The application does not describe an incremental reduction/increase in clock frequency. For example, the application does not describe skipping 1 out of 4 clock pulses, then 2 out of 4 clock pulses, then 3 out of 4 clock pulses, as illustrated in Durham in Figures 2, 3, or 4, or as described in column 3, line 50, through column 4, line 16. The application does not describe or suggest a state machine for switching between different levels. The clock frequency therefore must be adjusted non-incrementally.

B. Whether claims 1, 3, 4, 6, 7, and 9 have been erroneously rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

It is the Examiner's position that the specification does not explicitly teach adjusting the clock frequency non-incrementally.

Appellant respectfully disagrees. One of ordinary skill in the art reading the application as a whole understands that the application as originally filed describes a clock frequency that is adjusted non-incrementally.

The application describes a frequency regulating circuit that compares an instantaneous current consumption with a threshold value. If the instantaneous current consumption is lower than the threshold value, individual clock pulses pass through, and if the instantaneous current consumption is higher, the individual clock pulses are suppressed. The frequency regulating circuit adjusts the clock frequency immediately.

The application does not describe an incremental reduction/increase in clock frequency. For example, the application does not describe skipping 1 out of 4 clock pulses, then 2 out of 4 clock pulses, then 3 out of 4 clock pulses, as illustrated in Durham in Figures 2, 3, or 4, or as described in column 3, line 50, through column 4, line 16. The application does not describe or suggest a state machine for switching between different levels. The clock frequency therefore must be adjusted non-incrementally.

C. Whether claims 1, 3, 4, 6, 7, and 9 have been erroneously rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

It is the Examiner's position that the term "non-incrementally" is indefinite.

Appellant respectfully disagrees. "Incrementally" is well known to mean something performed in a series of regular additions or contributions, and thus "non-incrementally" must mean something performed that is not in a series of regular additions or contributions. Therefore,

adjusting a clock frequency instantaneously and non-incrementally must mean that the clock frequency is adjusted instantaneously in a single step. The term "non-incrementally" is therefore not indefinite.

D. Whether claims 1, 3, 4, 6, 7, and 9 have been erroneously rejected under 35 U.S.C. 103(a) as being unpatentable over Durham et al. (US 5,761,517; hereinafter "Durham") in view of Wang (US 5,943,203).

1. Independent claim 1 and dependent claim 3:

Independent claim 1 recites "A frequency regulating circuit ... comprising ... a pulse filter ... configured to suppress at least one clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input, such that said control device adjusts said clock frequency instantaneously and non-incrementally to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit."

The clock pulse is suppressed in response to the control signal such that the control device adjusts the clock frequency instantaneously and non-incrementally, and therefore the frequency regulating circuit of independent claim 1 has a fast reaction time. As soon as current consumption exceeds a predefined threshold value, at least one clock pulse is suppressed. During this suppression there is no longer a load. A brief time later the current consumption falls below the threshold value, and the clock pulse suppression is stopped. This process can be repeated again and again depending on the current profile. There is only full frequency mode (i.e., no clock pulse suppression) or no frequency mode (i.e., clock pulse suppression), and nothing in between (e.g., 3 clock pulses passed, 5 suppressed, 2 passed, 3 suppressed, etc.).

In contrast, Durham's circuit has the clock frequency is adjusted incrementally.

Referring to Durham's Figures 1A and 1B, Durham's circuit changes the output of an oscillator clock 27 prior to its input to dynamic logic circuit elements as a system clock signal 20.

The oscillator clock signal is controlled based upon a signal generated by a sensor 18 that determines the power consumption of the integrated circuit. The frequency of the clocked signal 20 is reduced/increased incrementally (explained below) based upon the determined level of power consumption. A pattern generator 17 inputs a digital signal to a series of interconnected registers 10, 11, 12, 13 which make up a loadable shift register. The output of the pattern generator 17 is based upon the input from the sensor 18. The bits shifted through the shift register are ANDed 7 with the oscillator clock signal to control the frequency of the system clock 20. Durham's frequency levels are therefore not adjusted directly in response to a control signal, as required by independent claim 1.

Regarding the incremental reduction/increase of frequency, Durham has defined frequency levels 4, 3, 2, 1, 0. See Durham, Figure. 2. Level 4 represents the speed of the system clock 20 equaling the speed of the oscillator clock 27. Level 3 represents the speed of the system clock 20 being 75% of the speed of the oscillator clock 27, that is 3/4 clock pulses passing. Level 2 represents the speed of the system clock 20 being 50%, that is 2/4 clock pulses passing. Level 1 represents the speed of the system clock 20 being 25%, that is 1/4 clock pulses passing. Level 0 represents no clock pulses passing, that is when the system is turned off. See Durham, Figure 4. This frequency increase/decrease happens incrementally using the shift register shown in Figures 1A and 1B and described above. As illustrated in Figure 4, the frequency levels can not be changed from level 4 to level 1 instantaneously. The frequency level increase/decrease happens gradually, making Durham's reaction time significantly slower than that of the circuit of independent claim 1. Durham therefore does not disclose adjusting the clock frequency instantaneously and non-incrementally, as required by independent claim 1.

Wang fails to make up for Durham's deficiencies.

Independent claim 1 and dependent claim 3 are therefore patentable over the applied references for at least these reasons.

2. Independent claim 4 and dependent claim 6:

Since independent claim 4 includes limitations similar to the limitations discussed above with respect to independent claim 1, independent claim 4 and its dependent claim 6 are patentable over the applied references for at least the same reasons.

3. Independent claim 7 and dependent claim 7:

Since independent claim 7 includes limitations similar to the limitations discussed above with respect to independent claim 1, independent claim 7 and its dependent claim 9 are patentable over the applied references for at least the same reasons.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto in the Claims Appendix.

X. EVIDENCE

As indicated in the Evidence Appendix, no evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

As indicated in the Related Proceedings Appendix, no related proceedings are referenced in II. above.

Please charge any fee, except for the Issue Fee, that may be necessary for the continued pendency of this application to our Deposit Account No. 50-2215.

Dated: October 1, 2010

Respectfully submitted,

By 

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CLAIMS APPENDIX

Claims 1, 3, 4, 6, 7, and 9 are on Appeal

1. A frequency regulating circuit for the current-consumption-dependent clock supply of a circuit configuration, comprising:

a current measuring device configured to measure an instantaneous current consumption of the circuit configuration;

means for comparing the instantaneous current measured by said current measuring device with a definable threshold value;

a controllable clock supply circuit having:

an output to be connected to a clock input of the circuit configuration;

a clock generator configured to generate a clock signal with clock pulses, said clock generator configured to generate a constant maximum internal frequency; and

a pulse filter configured to filter clock pulses from said clock signal from said clock generator, said pulse filter including a control input, a filtered clock signal being provided to said output;

a control device connected to said clock supply circuit and driving said clock supply circuit based upon the measured current consumption, said control device providing a control signal to said control input of said pulse filter when said means for comparing determine that the instantaneous current consumption exceeds the definable threshold value; and

said pulse filter configured to suppress at least one clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input, such that said control device adjusts said clock frequency instantaneously and non-incrementally to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit.

3. The frequency regulating circuit according to claim 1, wherein said means for comparing further comprise a comparator configured to compare the current measured by the current measuring device with the definable threshold value.

4. A frequency regulating circuit for the current-consumption-dependent clock supply of a circuit configuration, comprising:

a current measuring device configured to measure an instantaneous current consumption of the circuit configuration;

means for comparing the instantaneous current measured by said current measuring device with a definable threshold value;

a controllable clock supply circuit having:

an output to be connected to a clock input of the circuit configuration;

generator configured to generate a constant maximum internal frequency; and

a pulse filter connected to at least one of said clock generator and said output, configured to filter clock pulses from said clock signal from said clock generator, said pulse filter including a control input, a filtered clock signal being provided to said output;

a control device connected to said clock supply circuit and configured to drive said clock supply circuit based upon the measured current consumption, said control device programmed to provide a control signal to said control input of said pulse filter when said means for comparing determines that the instantaneous current consumption exceeds the definable threshold value; and

said pulse filter configured to suppress at least one clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input, such that, said control device adjusts said clock frequency instantaneously and non-incrementally to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit.

6. The frequency regulating circuit according to claim 4, wherein said means for comparing comprise a comparator configured to compare the current measured by the current measuring device with a definable threshold value.

7. A frequency regulating circuit for the current-consumption-dependent clock supply of a circuit configuration, comprising:

a current measuring device configured to measure an instantaneous current consumption of the circuit configuration;

means for comparing the instantaneous current measured by said current measuring device with a definable threshold value;

a controllable clock supply circuit having:

an output to be connected to a clock input of the circuit configuration;

a clock generator configured to generate a clock signal with clock pulses, said clock generator generating a constant maximum internal frequency; and

a pulse filter connected between said clock generator and said output, said pulse filter including a control input;

a control device connected to said clock supply circuit and configured to drive said clock supply circuit based upon the measured current consumption, said control device programmed to provide a control signal to said control input of said pulse filter when said means for comparing determine that the instantaneous current consumption exceeds the definable threshold value; and

said pulse filter configured to filter out at least one clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input, such that, said control device adjusts said clock frequency instantaneously and non-incrementally to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit.

9. The frequency regulating circuit according to claim 7, wherein said means for comparing comprise a comparator configured to compare the current measured by the current measuring device with a definable threshold value.

EVIDENCE APPENDIX

All evidence is in the record.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings for this matter.